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FIG. 1

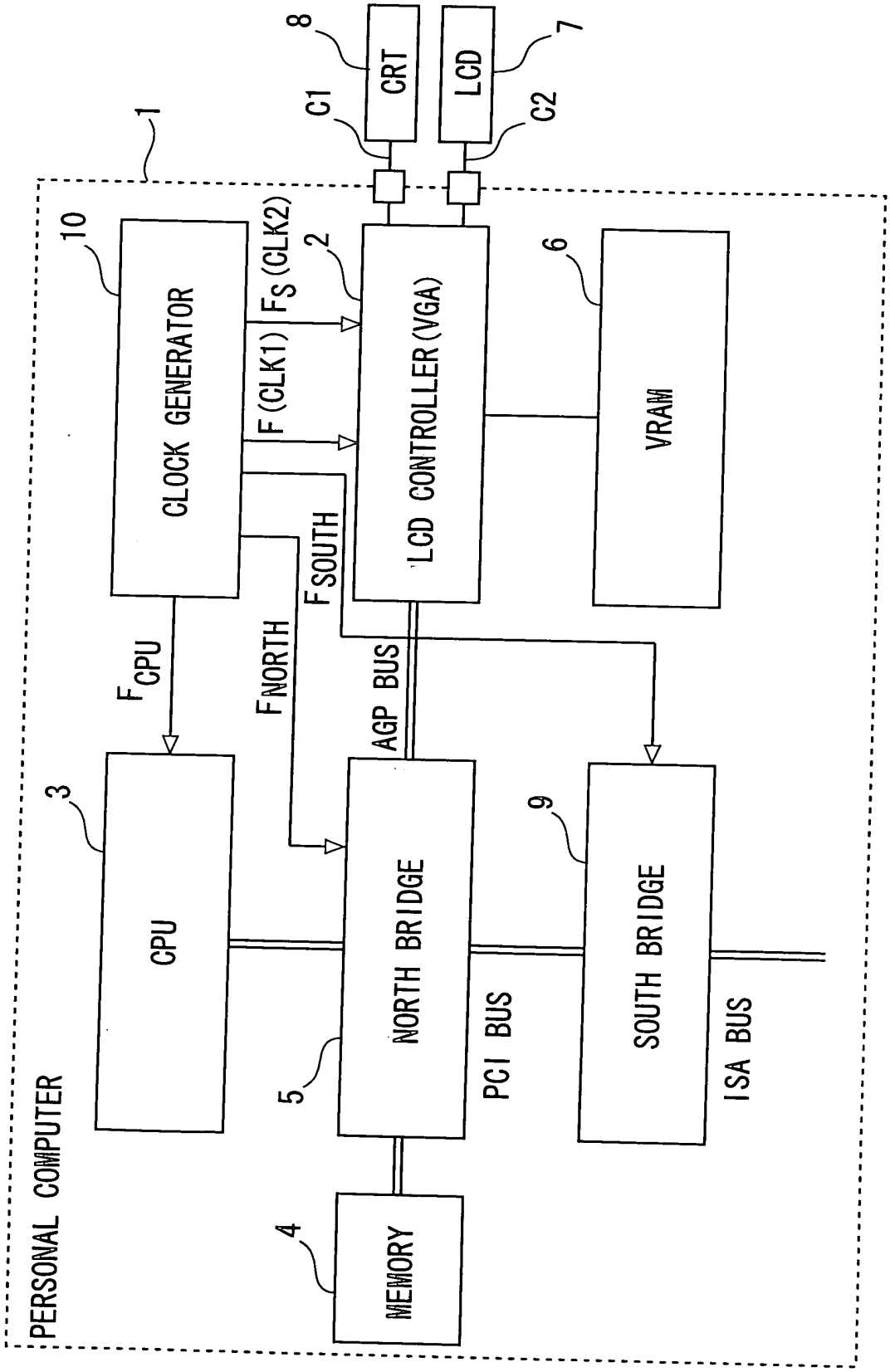
PERSONAL COMPUTER
1
CRT
8
LCD
7
C1
C2
CLOCK GENERATOR
10
FS (CLK2)
F (CLK1)
LCD CONTROLLER (VGA)
2
VRAM
6
FSOUTH
FCPU
FNORTH
AGP BUS
CPU
3
NORTH BRIDGE
5
SOUTH BRIDGE
9
PCI BUS
ISA BUS
MEMORY
4

FIG. 2

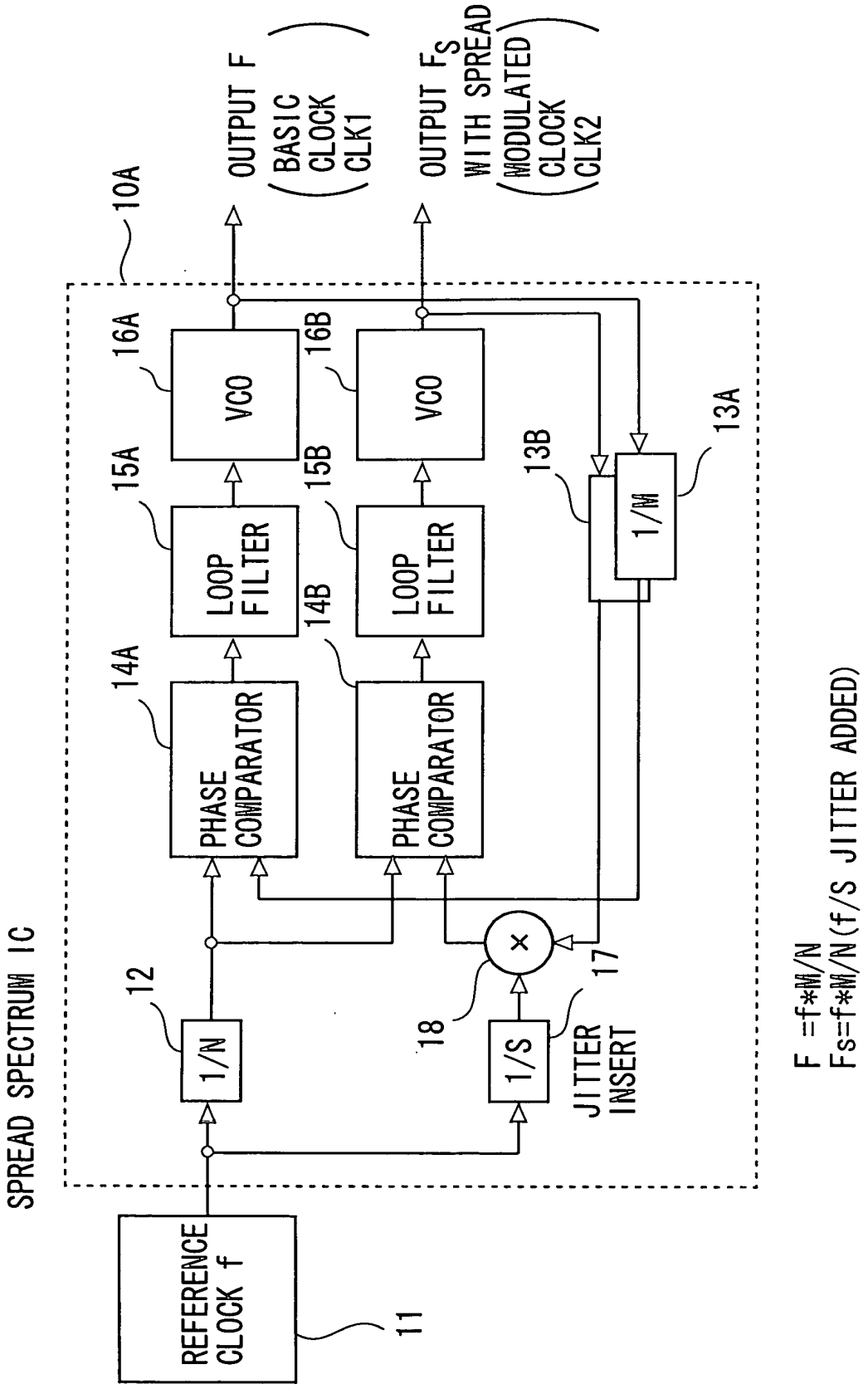
SPREAD SPECTRUM IC
10A
REFERENCE CLOCK f
11
1/N
12
PHASE COMPARATOR
14A
PHASE COMPARATOR
14B
LOOP FILTER
15A
LOOP FILTER
15B
VCO
16A
VCO
16B
OUTPUT F (BASIC CLOCK CLK1)
OUTPUT Fs WITH SPREAD (MODULATED CLOCK CLK2)
1/M
13A
13B
×
17
18
1/S
JITTER INSERT
F =f*M/N
Fs=f*M/N(f/S JITTER ADDED)

FIG. 3A

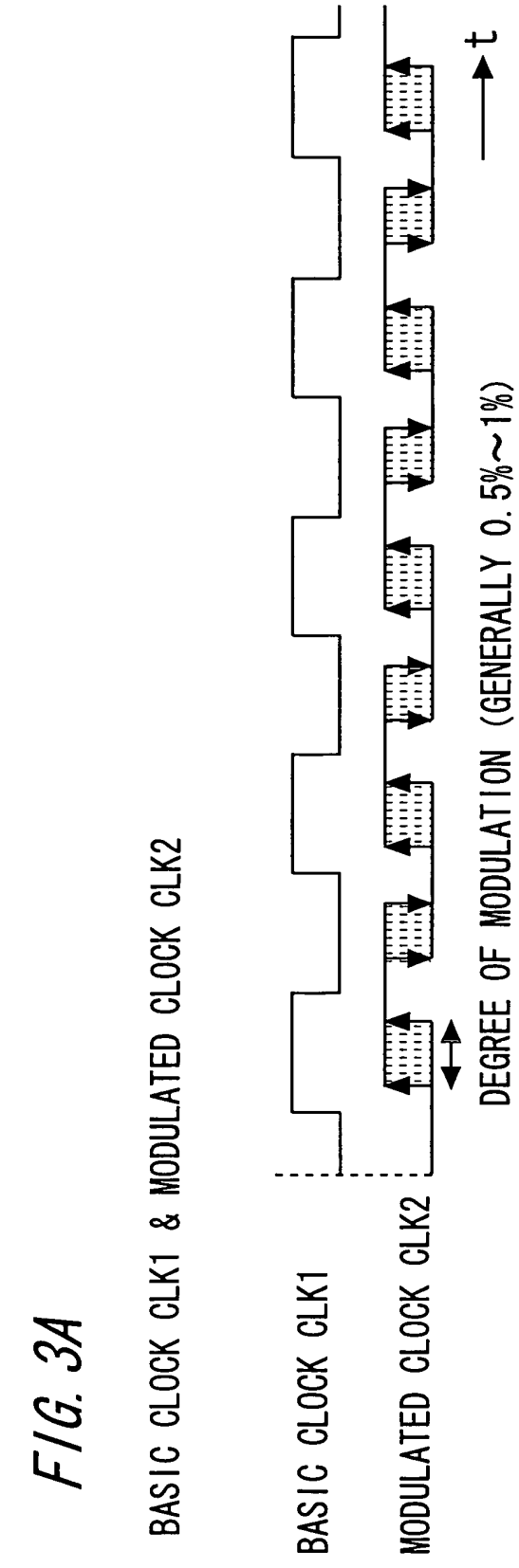
BASIC CLOCK CLK1 & MODULATED CLOCK CLK2
BASIC CLOCK CLK1
MODULATED CLOCK CLK2
DEGREE OF MODULATION (GENERALLY 0.5%~1%)
t

FIG. 3B

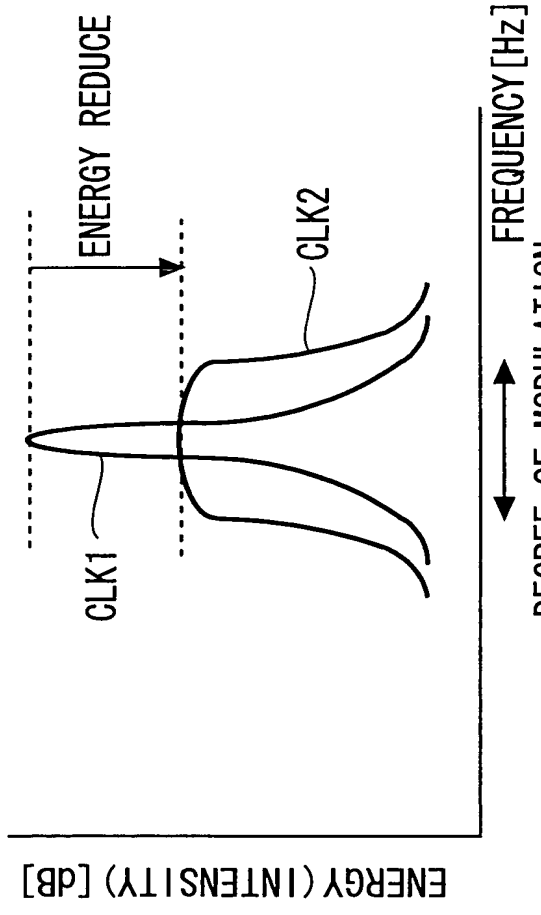
ENERGY (INTENSITY) [dB]
ENERGY REDUCE
CLK1
CLK2
FREQUENCY [Hz]
DEGREE OF MODULATION

FIG. 4

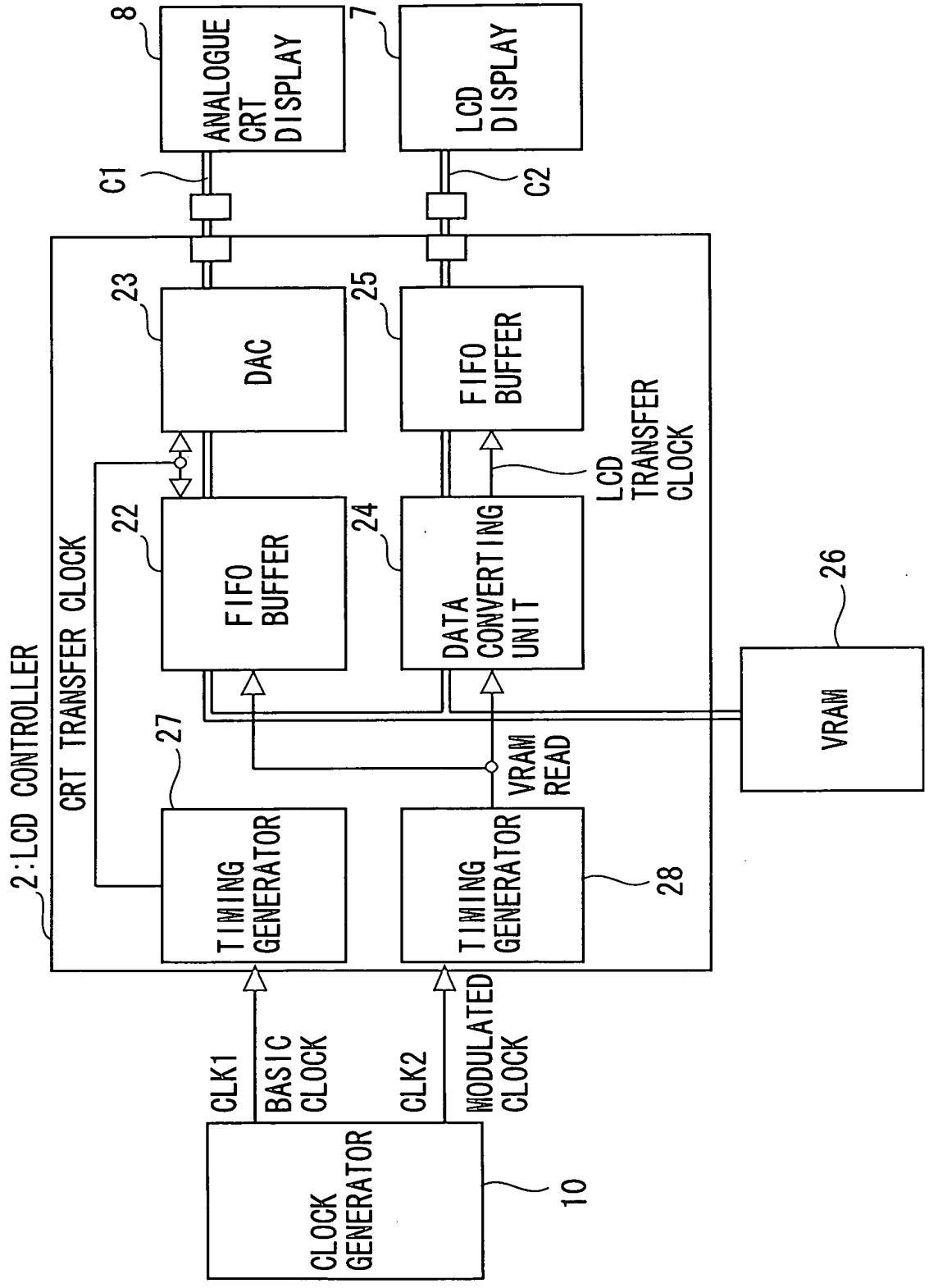
8
ANALOGUE CRT DISPLAY
7
LCD DISPLAY
C1
C2
23
DAC
25
FIFO BUFFER
LCD TRANSFER CLOCK
22
FIFO BUFFER
24
DATA CONVERTING UNIT
26
VRAM
2:LCD CONTROLLER
CRT TRANSFER CLOCK
27
TIMING GENERATOR
VRAM READ
TIMING GENERATOR
28
CLK1
BASIC CLOCK
CLK2
MODULATED CLOCK
CLOCK GENERATOR
10

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FIG. 5

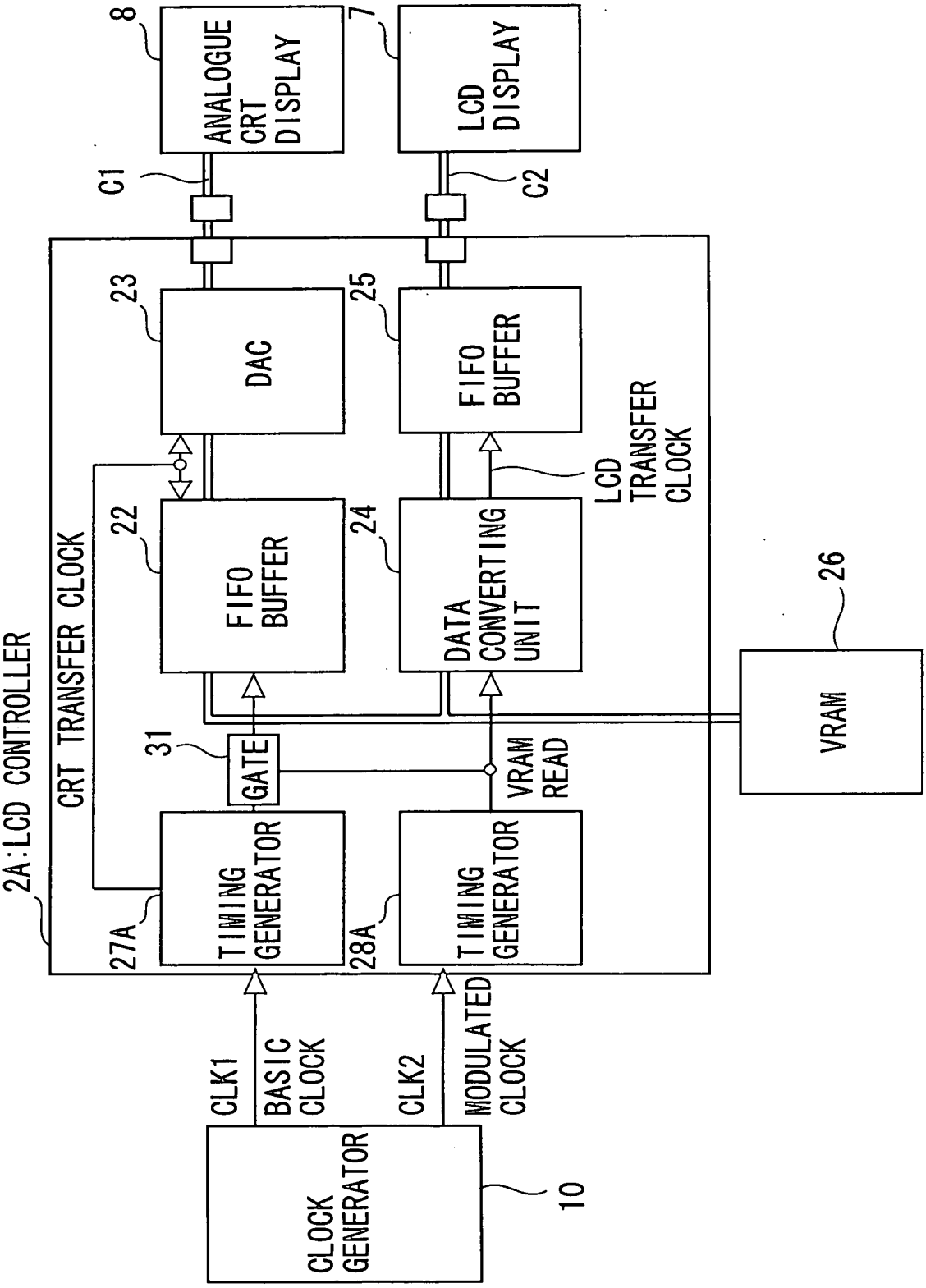
8
ANALOGUE CRT DISPLAY
7
LCD DISPLAY
C1
C2
23
DAC
25
FIFO BUFFER
LCD TRANSFER CLOCK
22
FIFO BUFFER
24
DATA CONVERTING UNIT
26
VRAM
31
GATE
VRAM READ
2A:LCD CONTROLLER
CRT TRANSFER CLOCK
27A
TIMING GENERATOR
28A
TIMING GENERATOR
CLK1
BASIC CLOCK
CLK2
MODULATED CLOCK
CLOCK GENERATOR
10

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FIG. 6

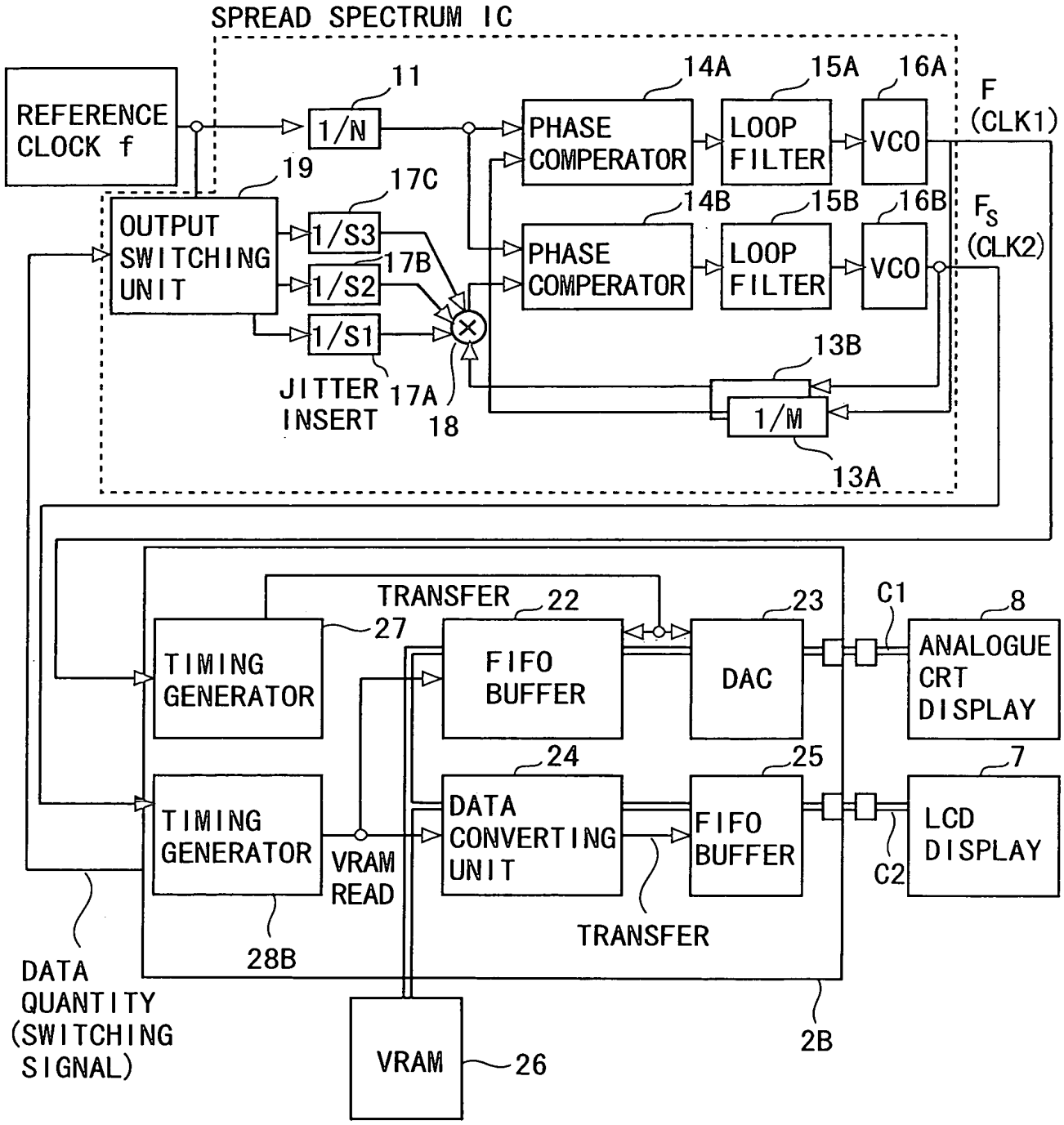
SPREAD SPECTRUM IC
REFERENCE CLOCK f
11
1/N
14A
15A
16A
PHASE COMPERATOR
LOOP FILTER
VCO
F (CLK1)
19
17C
OUTPUT SWITCHING UNIT
1/S3
14B
15B
16B
17B
1/S2
PHASE COMPERATOR
LOOP FILTER
VCO
Fs (CLK2)
1/S1
13B
JITTER INSERT
17A
18
1/M
13A
TRANSFER
22
23
C1
8
27
TIMING GENERATOR
FIFO BUFFER
DAC
ANALOGUE CRT DISPLAY
24
25
7
TIMING GENERATOR
DATA CONVERTING UNIT
FIFO BUFFER
LCD DISPLAY
VRAM READ
C2
TRANSFER
28B
DATA QUANTITY (SWITCHING SIGNAL)
2B
VRAM
26

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FIG. 7

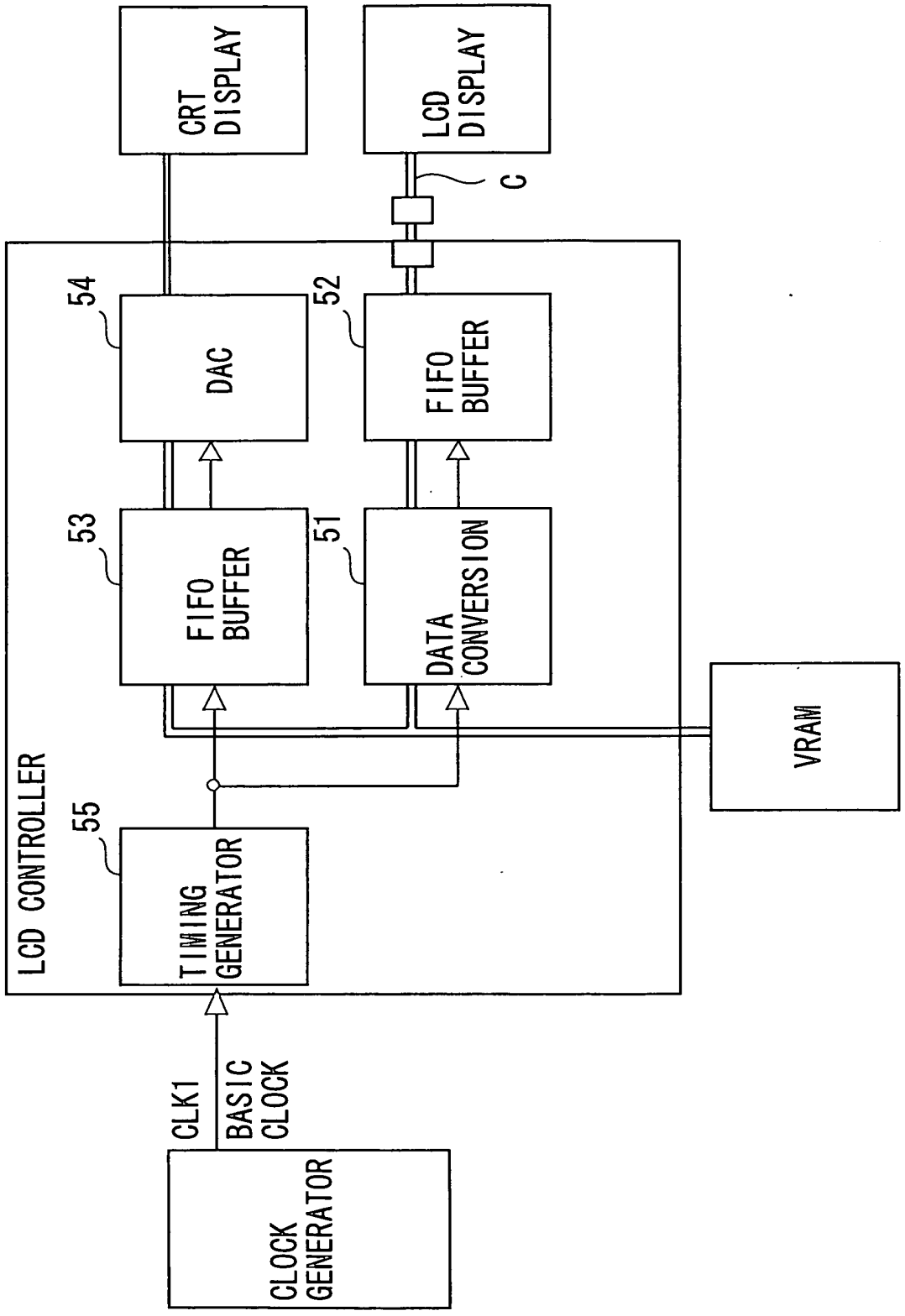
CRT DISPLAY
LCD DISPLAY
C
54
DAC
52
FIFO BUFFER
53
FIFO BUFFER
51
DATA CONVERSION
VRAM
LCD CONTROLLER
55
TIMING GENERATOR
CLK1
BASIC CLOCK
CLOCK GENERATOR

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FIG. 8A

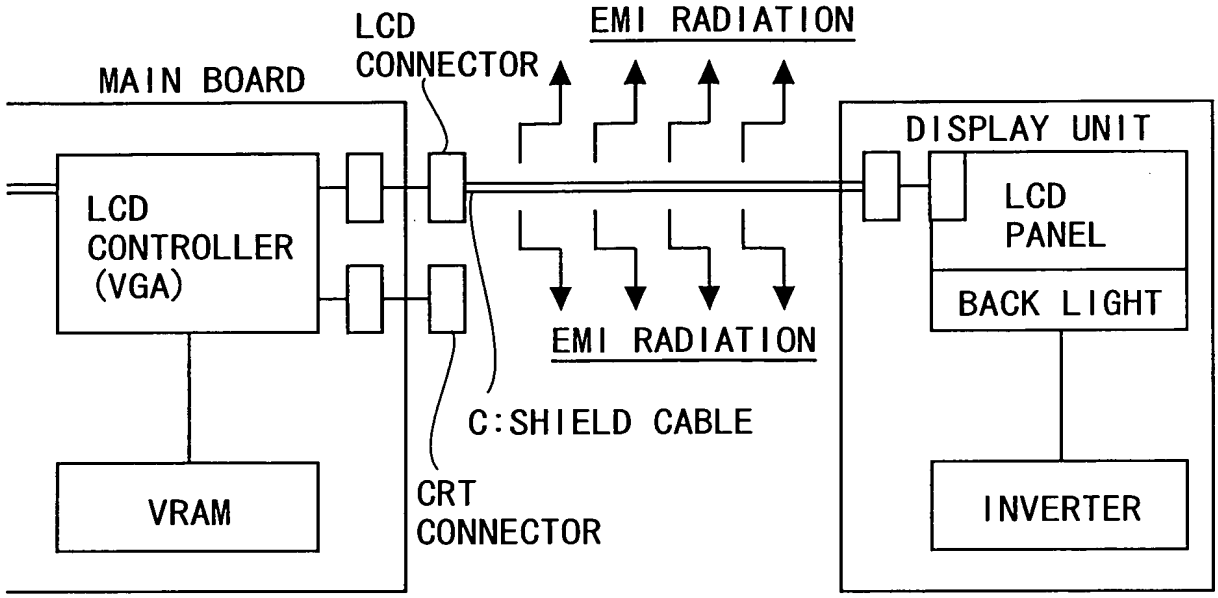

FIG. 8B

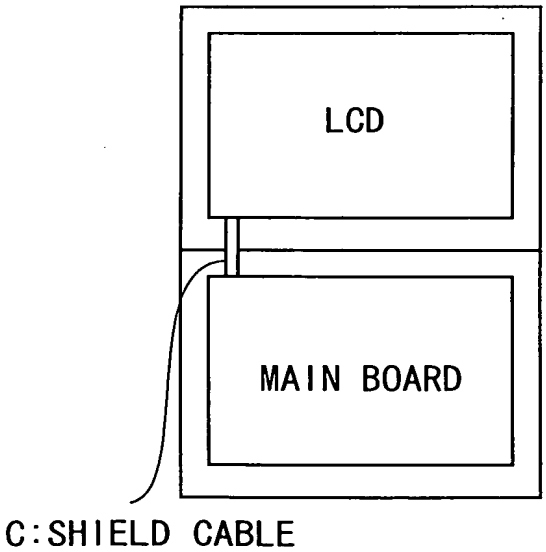
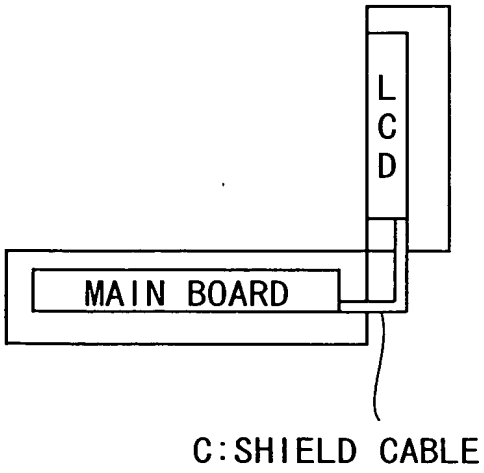
FIG. 8C